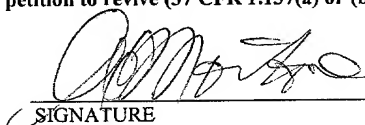


FORM PTO-1390 (REV. 9-2001)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER <b>520.41003X00 filed December 28, 2001</b>	
<b>TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371</b>					
INTERNATIONAL APPLICATION NO. <b>PCT/JP00/04141</b>		INTERNATIONAL FILING DATE <b>June 23, 2000</b>		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) <b>10/019407</b>	
PRIORITY DATE CLAIMED <b>June 28, 1999</b>					
TITLE OF INVENTION <b>POLYCRYSTALLINE SEMICONDUCTOR THIN FILM SUBSTRATE MANUFACTURING METHOD OF THE SAME, SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE</b>					
APPLICANT(S) FOR DO/EO/US <b>KIMURA, YOSHINOBU KAMO, TAKAHIRO KANEKO, YOSHIYUKI</b>					
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:					
<p>1. <input checked="" type="checkbox"/> This is a <b>FIRST</b> submission of items concerning a filing under 35 U.S.C. 371.</p> <p>2. <input type="checkbox"/> This is a <b>SECOND</b> or <b>SUBSEQUENT</b> submission of items concerning a filing under 35 U.S.C. 371.</p> <p>3. <input type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.</p> <p>4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31).</p> <p>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2))</p> <p>a. <input type="checkbox"/> is transmitted hereto (required only if not communicated by the International Bureau).</p> <p>b. <input checked="" type="checkbox"/> has been communicated by the International Bureau.</p> <p>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office(RO/US)</p> <p>6. <input checked="" type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).</p> <p>a. <input checked="" type="checkbox"/> is attached hereto.</p> <p>b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4).</p> <p>7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))</p> <p>a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau).</p> <p>b. <input type="checkbox"/> have been communicated by the International Bureau.</p> <p>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</p> <p>d. <input type="checkbox"/> have not been made and will not be made.</p> <p>8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</p> <p>9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</p> <p>10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).</p> <p><b>Items 11 to 20 below concern document(s) or information included:</b></p> <p>11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.</p> <p>12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.</p> <p>13. <input type="checkbox"/> A <b>FIRST</b> preliminary amendment.</p> <p>14. <input type="checkbox"/> A <b>SECOND</b> or <b>SUBSEQUENT</b> preliminary amendment.</p> <p>15. <input type="checkbox"/> A substitute specification.</p> <p>16. <input checked="" type="checkbox"/> A change of power of attorney and/or address letter.</p> <p>17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.</p> <p>18. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4).</p> <p>19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).</p> <p>20. <input checked="" type="checkbox"/> Other items or information: <b>PCT Request Form; International Publication No. WO 01/01464(cover sheet); International Preliminary Examination Report; International Search Report; Credit Card Payment Form; Figs. 1-9</b></p>					

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U.S. APPLICATION NO. (If known, see 37 CFR 1.5) <b>10/019407</b>		INTERNATIONAL APPLICATION NO. <b>PCT/JP00/04141</b>		ATTORNEY'S DOCKET NUMBER <b>520.41003X00</b>																																																																
<b>21. The following fees are submitted:</b> <b>BASIC NATIONAL FEE (37 CFR 1.492(a) (1) - (5)):</b> <input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO.....\$1040.00 <input checked="" type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....\$890.00 <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....\$740.00 <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....\$710.00 <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....\$100.00  <b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b> Surcharge of \$130.00 for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492(e)). <input type="checkbox"/> 20 <input type="checkbox"/> 30 <table border="1" style="width:100%; border-collapse: collapse;"><thead><tr><th>CLAIMS</th><th>NUMBER FILED</th><th>NUMBER EXTRA</th><th>RATE</th><th>\$</th></tr></thead><tbody><tr><td>Total Claims</td><td>20- 20 =</td><td>0</td><td>x \$18.00</td><td>\$0.00</td></tr><tr><td>Independent Claims</td><td>9- 3 =</td><td>6</td><td>x \$84.00</td><td>\$504.00</td></tr><tr><td colspan="3"></td><td>+ \$280.00</td><td>\$0.00</td></tr><tr><td colspan="4"><b>TOTAL OF ABOVE CALCULATIONS =</b></td><td>\$1394.00</td></tr><tr><td colspan="4"><input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.</td><td>\$0.00</td></tr><tr><td colspan="4"><b>SUBTOTAL =</b></td><td>\$1394.00</td></tr><tr><td colspan="4">Processing fee of \$130.00 for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492(f)).      <input type="checkbox"/> 20      <input type="checkbox"/> 30</td><td>\$0.00</td></tr><tr><td colspan="4"><b>TOTAL NATIONAL FEE =</b></td><td>\$1394.00</td></tr><tr><td colspan="4">Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property</td><td>\$0.00</td></tr><tr><td colspan="4"><b>TOTAL FEES ENCLOSED =</b></td><td>\$1394.00</td></tr><tr><td colspan="4"></td><td><b>Amount to be refunded:</b> \$</td></tr><tr><td colspan="4"></td><td><b>charged:</b> \$</td></tr></tbody></table>				CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	Total Claims	20- 20 =	0	x \$18.00	\$0.00	Independent Claims	9- 3 =	6	x \$84.00	\$504.00				+ \$280.00	\$0.00	<b>TOTAL OF ABOVE CALCULATIONS =</b>				\$1394.00	<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				\$0.00	<b>SUBTOTAL =</b>				\$1394.00	Processing fee of \$130.00 for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492(f)). <input type="checkbox"/> 20 <input type="checkbox"/> 30				\$0.00	<b>TOTAL NATIONAL FEE =</b>				\$1394.00	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property				\$0.00	<b>TOTAL FEES ENCLOSED =</b>				\$1394.00					<b>Amount to be refunded:</b> \$					<b>charged:</b> \$
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<p>a. <input type="checkbox"/> A check in the amount of \$_____ to cover the fees is enclosed.</p> <p>b. <input type="checkbox"/> Please charge my Deposit Account No. <b>01-2135</b> in the amount of \$_____ to cover the above fees. A duplicate copy of this sheet is enclosed.</p> <p>c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposition Account No. <b>01-2135</b>. A duplicate copy of this sheet is enclosed.</p> <p>d. <input checked="" type="checkbox"/> Fees are to be charged to a credit card. <b>WARNING:</b> Information on this form may become public. <b>Credit card information should not be included on this form.</b> Provide credit card information and authorization on PTO-2038.</p> <p><b>NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.</b></p> <p>SEND ALL CORRESPONDENCE TO: <b>Antonelli, Terry, Stout &amp; Kraus, LLP</b> 1300 North Seventeenth Street Suite 1800 Arlington, VA 22209 USA</p>																																																																				
				<div style="text-align: center;"> SIGNATURE <b>Gregory E. Montone</b> NAME <b>28,141</b> REGISTRATION NO.</div>																																																																

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## SPECIFICATION

POLYCRYSTALLINE SEMICONDUCTOR THIN FILM SUBSTRATE,  
MANUFACTURING METHOD OF THE SAME, SEMICONDUCTOR DEVICE  
AND ELECTRONIC DEVICE

## Technical Field

The present invention relates to a polycrystalline semiconductor thin film substrate, a manufacturing method thereof, a semiconductor device, a method of manufacturing a semiconductor device and an electronic apparatus and, more in particular, it relates to a technique which is effective to application use for manufacturing a transistor (thin film transistor: TFT) in a surface layer portion of a polycrystalline film (polycrystalline semiconductor thin film) and a manufacturing technique of a polycrystalline semiconductor thin film substrate for manufacturing the thin film transistor, as well as an electronic apparatus incorporated with the thin film transistor such as a liquid crystal display or data processor.

## Background Art

Thin film transistors (TFT) used for image displays in the prior art have been formed using, as a device material, polycrystalline silicon formed by a melting recrystallization method such excimer laser annealing from amorphous silicon or

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microcrystalline silicon formed by a plasma CVD process on an insulative substrate such as glass or quartz as a base material.

The semiconductor device (TFT) and the manufacturing method thereof in the prior art are to be described with reference to Fig. 17(a) to (d). As shown in Fig. 17(a), an amorphous silicon thin film 202 is deposited on one surface of a glass substrate 201.

Then, as shown in Fig. 17(b), when the surface of the amorphous silicon thin film 202 is scanned by a linear excimer laser beam 204 in the direction of an arrow 203, the amorphous silicon thin film 202 is heated by the excimer laser beam 204 and changed from an amorphous structure into a polycrystalline structure. When the entire surface of the amorphous silicon film 202 is heated by the excimer laser beam 204 under scanning, a polycrystalline silicon thin film 205 is formed as shown in Fig. 17(c). In Fig. 17(c), the polycrystalline silicon thin film 205 is made of silicon crystal grains and a grain boundary 206 is formed between the crystal grains.

The process described above is referred to as a laser heating process. This is adopted when a polycrystalline silicon thin film at high quality is prepared on a substrate comprising a low melting material such as glass. They are described in details, for example, in "1996 Society for Information Display International Symposium Digest of Technical Papers, pp 17 - 29" and "IEEE Transactions on Electron Devices, vol. 43, No. 9, 1996,

pp 1454 to 1458" and the like.

Fig. 17(d) shows a transistor (TFT) formed by using the polycrystalline silicon thin film in Fig. 17(c).

A gate insulation film 208 such as a silicon oxide film is disposed on the polycrystalline silicon thin film 205. Further, a source impurity implantation region 207 and a drain impurity implantation region 206 are formed on the polycrystalline silicon thin film 205. A thin film transistor is formed by disposing a gate electrode on the source - impurity implantation regions 207 and 209 and the gate insulation film 208.

Fig. 18 shows the dependence of the size of the silicon crystal grain and the roughness of the polycrystalline silicon thin film on the irradiation laser energy in the prior art (dependence 301 of the size of the crystal grain on the laser energy density). Silicon is not crystallized at the energy with a laser energy density of  $200 \text{ mJ/cm}^2$  or less but crystallization initiates when it exceeds  $200 \text{ mJ/cm}^2$  and the size of the crystal grain increases along with an increase in the laser energy density.

However, when the laser energy density exceeds  $250 \text{ mJ/cm}^2$ , the silicon crystal grain becomes smaller. Since a polycrystalline silicon thin film transistor having favorable characteristics may be manufactured by increasing the size of the silicon crystal grains, the energy density of the laser is

set to 250 mJ/cm<sup>2</sup>.

The value of the laser energy density in the prior art may sometimes vary since it depends on the nature of the amorphous silicon film (for example, growing method, film thickness). They are described in details, for example, in "Applied Physics Letters, vol. 63, No. 14, 1993, pp 1969 - 1971".

Further, for increasing the grain diameter of the crystal grains, laser irradiation may preferably be conducted by heating the substrate at 400°C. This is because the solidification velocity is lowered by heating the substrate and the grain diameter increases up to about 500 nm. Further, since a temperature gradient is caused at the end of the laser beam, the size of the crystal grains varies remarkably. In order to prevent this, laser may be preferably irradiated under overlapping. They are reported in "Proceedings of The Institute of Electronics, Information and Communication Engineers C-II Vol. J76-C-II, 1993, pp 241-248".

Further, for making the size of the crystal grains uniform, first laser irradiation is applied at first at a low energy density and, subsequently, a second laser irradiation is applied at a high energy density required for crystallization. Such a two-step laser irradiation is applied for forming crystal seeds by the first laser irradiation and crystallization of them by the second laser irradiation. In this case, while the uniformness is improved, the crystal grain diameter is reduced.

This is reported in "Proceedings of 42th Laser Materials Processing Conference, 1997, pp. 121 - 130".

#### Disclosure of the Invention

It has been found that the prior art described above involves the following problems.

When many grain boundaries are present in a silicon channel region under a gate electrode, non-uniformness thereof may sometimes lower the carrier mobility  $\mu$  to several  $\text{cm}^2/\text{V}\cdot\text{s}$ , for example, due to the variation of conduction carriers.

Further, when the grain boundaries present in the silicon channel region under the gate electrode varies in density, a threshold voltage  $V_{th}$  varies up to several V in individual transistors.

In addition, when the crystal grain in the silicon channel region under the gate electrode varies in size, individual transistors vary in carrier mobility  $\mu$ .

Further, when roughness of the grain boundaries is present in the silicon channel region under the gate electrode, individual transistors vary and degrade in performance.

Further, when impurities are implanted in the polycrystal region, since impurities segregate in the grain boundaries, it is difficult to control the carrier concentration.

The present inventors have made observation and studies

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on the distribution of crystal grains of polycrystal semiconductor thin films manufactured in the prior art. Fig. 19 shows the arrangement of crystal grains of the polycrystalline semiconductor thin film in the existent polycrystalline semiconductor thin film substrate used for the manufacture of thin film transistors.

This figure is based on microscopic photography and crystal grains 250 are in various shapes such as trigonal, tetragonal, pentagonal, hexagonal, heptagonal and octagonal shapes, in which hexagonal crystal grains 251 are most predominant. It has been found that the number of the hexagonal grains 251 is about 30 to 40%. A square region of 10  $\mu\text{m}$  side is taken as an evaluation region and observation was made at an optional place.

The present inventors have considered that the crystal grains can be unified in the polycrystal semiconductor thin film, that is, the characteristics of the thin film transistor can be improved and unified by decreasing the number of trigonal, square and pentagonal shapes and increasing the number of hexagonal crystal grains by so much.

Then, when a relation between the energy density of the laser irradiated to the amorphous silicon film and the shape of the crystal grains formed was examined, it has been found that there exists a laser energy density on every shape that maximizes the formation of each shape (suitable shape selection



laser energy density  $E_c$ ). That is, it has been found that there exist laser energy density that maximizes formation of the tetragonal shape, the laser energy density that maximizes formation of the pentagonal shape and the laser energy density that maximizes formation of the hexagonal shape.

This invention is an invention adopting a crystallization method based on the suitable shape selection laser energy density  $E_c$  by the finding described above, which defines the crystal grains in the polycrystalline semiconductor thin film as the hexagonal shape and defines the rate of the hexagonal shape to 50 - 100%.

An object of this invention is to provide a polycrystalline semiconductor thin film in which the size of the crystal grains and the carrier concentration are uniform and which has a planar surface.

Another object of this invention is to provide a semiconductor device having a thin film transistor with favorable characteristics and with less variation in characteristics.

A further object of this invention is to provide an electronic apparatus with favorable characteristics incorporated with a semiconductor device having a thin film transistor.

The foregoing and other objects, as well as novel features of this invention will become apparent with reference to the descriptions of the specification and the appended

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drawings.

Outline of typical inventions among those disclosed in the present application will be described simply as below.

The means (1) described above provides a polycrystal semiconductor thin film substrate comprising an insulative substrate and a polycrystalline semiconductor thin film disposed on one surface of the insulative substrate, in which 50 - 100% of the crystal grains forming the polycrystalline semiconductor thin film are of a hexagonal shape. Electron orbits of the crystal grains at the surface and inside the polycrystalline semiconductor thin film are bonded to each other. The roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less. The insulative substrate is a glass substrate and the polycrystalline semiconductor thin film is a polycrystalline silicon film.

Such a polycrystalline semiconductor thin film substrate is manufactured by the following method. In a method of manufacturing a polycrystalline semiconductor thin film substrate by forming an amorphous semiconductor film on the surface of an insulative substrate, then irradiating the amorphous semiconductor film with a laser beam to crystallize the amorphous semiconductor film to form a polycrystalline semiconductor thin film, a UV-ray is irradiated to the rear face of the insulative substrate or to the amorphous semiconductor film thereby to heat the amorphous semiconductor film to a

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melting temperature or lower, and a laser beam at a suitable shape selection laser energy density  $E_c$  which maximizes formation of the crystal grains hexagonal shape is irradiated repeatedly to the surface of the amorphous semiconductor film, thereby converting it into the polycrystalline semiconductor thin film.

After repeating a first laser irradiation for multiple cycles at the suitable shape selection laser energy density  $E_c$  to the surface of the amorphous semiconductor film, a second laser irradiation is repeated for multiple cycles at an energy density lower than that of the laser energy density  $E_c$ . The first laser irradiation and the second laser irradiation are conducted while scanning the laser beam along the surface of the amorphous semiconductor film. The irradiation is conducted while synchronizing the period of the laser beam irradiation and the period of the UV-ray heating. The laser beam irradiation is conducted by an excimer laser and the laser beam emitted from the excimer laser is divided by an optical component into two optical channels, such that one of them reaches a laser beam irradiation position with a delay and the laser beam passing through a shorter optical channel length is attenuated by being passed through an optical attenuator and caused to reach the laser beam irradiation position, thereby forming the polycrystalline semiconductor thin film.

(2) A semiconductor device in which plural transistors

are formed to a polycrystalline semiconductor thin film wherein the transistor (thin film transistor) is formed to a polycrystal semiconductor thin film of the constitution (1) described above.

The semiconductor device as described above is manufactured by the following method. It is manufactured by a method of manufacturing a semiconductor device by forming plural transistors in a polycrystalline semiconductor thin film wherein the polycrystalline semiconductor thin film has the constitution (1) described above.

(3) An electronic apparatus incorporating a semiconductor device in which plural transistor are formed in a polycrystal semiconductor thin film, wherein the semiconductor device is made up with the semiconductor device of the constitution (2) described above. For example, the electronic apparatus is a liquid crystal display, and the semiconductor device has transistors for operating each of pixels of a liquid crystal display panel and transistors constituting the peripheral driver circuitries and is attached being overlapped to a liquid crystal display panel of the liquid crystal display.

(4) An electronic apparatus incorporating a semiconductor device in which plural transistors are formed in a polycrystalline semiconductor thin film, wherein the electronic apparatus is, for example, a data processor in which a central processing unit, a cash circuitry, a memory circuitry, a peripheral circuitry, an input/output circuitry and a bus

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circuitry are formed with each of the transistors of the semiconductor device.

According to the constitution (1) described above, (a) since 50 to 100% of the crystal grains in the polycrystalline semiconductor thin film comprise hexagonal crystal grains and the grain diameter is uniform as from 0.2 to 0.3  $\mu\text{m}$ , a substrate with improved carrier mobility  $\mu$  and with less variation in the carrier mobility  $\mu$  in each of the regions can be provided.

(b) Since the electron orbits of the grain boundaries at the surface and inside the polycrystalline semiconductor thin film are bonded to each other, it is possible to provide an effect of making the carrier mobility constant and improving the reliability of individual transistors. That is, longer life can be attained for individual transistors.

(c) Since the laser beam is irradiated repeatedly upon formation of the polycrystalline semiconductor thin film, roughness on the surface of the polycrystalline semiconductor thin film can be reduced to provide a planar polycrystalline semiconductor thin film substrate.

(d) Since laser beam irradiation is conducted repeatedly by multiple cycles at the suitable shape selection laser energy density  $E_c$  most preferred for forming the hexagonal shape, hexagonal shape crystals are formed successively in the amorphous semiconductor film, adjacent hexagonal crystal grains move to each other and are gradually in close contact with

adjacent hexagonal crystal grains. Subsequently, since laser beam irradiation is conducted repeatedly for multiple cycles at a laser energy density lower than the suitable shape selection energy density  $E_c$ , impurities less segregate to the grain boundaries to make the carrier concentration of the crystal grains constant.

According to the constitution (2) described above, (a) since 50 to 100% of the crystal grains comprise hexagonal crystal grains and the grain size thereof is uniform as 0.2 to 0.5  $\mu\text{m}$  in the polycrystalline semiconductor thin film, when a transistor (TFT) is formed, the grain boundaries are reduced in the silicon channel region under the gate electrode, the carrier mobility  $\mu$  is improved and variation in the carrier mobilities is decreased in each of the transistors.

(b) In each of the transistors, the density of the grain boundaries present in the silicon channel region below the gate electrode less varies and the threshold voltage  $V_{th}$  is made uniform in each of the transistors.

(c) Since the laser beam is irradiated repeatedly upon forming the polycrystalline semiconductor thin film, roughness on the surface of the polycrystalline semiconductor thin film is reduced and variation in the performance of individual transistors is reduced and degradation less occurs to attain the longer life of the transistors.

(d) In the formation of the polycrystalline

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semiconductor thin film, since laser beam irradiation is conducted repeatedly for multiple cycles at the suitable shape selection laser energy density  $E_c$  most preferred for forming the hexagonal shape, hexagonal seed crystals are formed successively in the amorphous semiconductor film, adjacent hexagonal crystal grains move to each other and are gradually in close contact with adjacent hexagonal crystal grains. Subsequently, since laser beam irradiation is conducted repeatedly for multiple cycles at a laser energy density lower than the suitable shape selection energy density  $E_c$ , impurities less segregate to the grain boundaries to make the carrier concentration of the crystal grains constant. As the result characteristics of the transistors become stable.

According to the constitutions (3) described above, since each of plural transistors for operating each of pixels on the liquid crystal display panel is made uniform in the characteristics, image at high quality can be obtained.

According to the constitution (4) described above, since the central processing unit, the cash circuitry, the memory circuitry, the peripheral circuitry, the input/output circuitry and the bus circuitry are formed with the thin film transistors formed on the glass substrate surface, it is possible to provide a data processor of reduced thickness and higher performance.

Brief Description of Drawings

Fig. 1 is a schematic cross sectional view illustrating a state of manufacturing a polycrystalline semiconductor thin film according to an embodiment (Embodiment 1) of the present invention.

Fig. 2 is a schematic cross sectional view illustrating a method of manufacturing a polycrystalline semiconductor thin film of Embodiment 1.

Fig. 3 is a perspective view of a polycrystalline semiconductor thin film substrate of Embodiment 1.

Fig. 4 is a partial cross sectional view of a polycrystalline semiconductor thin film substrate of Embodiment 1.

Fig. 5 is a schematic plan view illustrating the constitution of crystal grains in a polycrystalline semiconductor thin film of a polycrystalline semiconductor thin film substrate of Embodiment 1.

Fig. 6 illustrates a group of graphs showing the result of analysis such as properties of crystal grains and difference in the manufacturing conditions in the manufacture of a polycrystalline semiconductor thin film.

Fig. 7 is a graph showing a correlation between hexagonal crystal grains and the number of cycles of laser beam irradiation in the manufacture of a polycrystalline semiconductor thin film and a graph illustrating a relation between the number of cycles of laser beam irradiation and the



roughness on the surface of a polycrystalline semiconductor thin film.

Fig. 8 is a schematic view illustrating the difference of crystal grains depending on the difference in a laser energy density.

Fig. 9 is a schematic view illustrating the growing process of crystal grains by laser beam irradiation applied repeatedly.

Fig. 10 is a schematic cross sectional view illustrating a transistor (thin film transistor) manufactured according to Embodiment 1.

Fig. 11 is a schematic cross sectional view illustrating a method of manufacturing a thin film transistor according to Embodiment 1.

Fig. 12 is a schematic cross sectional view illustrating the state of manufacturing a polycrystalline semiconductor thin film according to another embodiment (Embodiment 2) of the present invention.

Fig. 13 is a schematic cross sectional view illustrating the state of manufacturing a polycrystalline semiconductor thin film according to another embodiment (Embodiment 3) of the present invention.

Fig. 14 is a schematic perspective view illustrating a portion of a liquid crystal display according to another embodiment (Embodiment 4) of the present invention.

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Fig. 15 is a schematic perspective view illustrating a portion of a data processor according to another embodiment (Embodiment 5) of the present invention.

Fig. 16 is an enlarged schematic view of a portion surrounded with a dotted chain in Fig. 15.

Fig. 17 is a schematic cross sectional view illustrating an existent method of manufacturing a thin film transistor.

Fig. 18 is a diagram illustrating a correlation between the laser energy density and the crystal grain diameter in the prior art.

Fig. 19 is a schematic view illustrating a constitution of crystal grains of a polycrystalline semiconductor thin film in an existent polycrystalline semiconductor thin film substrate.

#### Best Mode for Carrying Out the Invention

Hereinafter, preferred embodiments of this invention will be described with reference to the drawings, in which like or corresponding parts are denoted by the same reference characters and the duplicate description thereof will be omitted.

#### Embodiment 1

Fig. 1 to Fig. 11 are views concerning the manufacturing technique of a semiconductor device having a thin film transistor as an embodiment (Embodiment 1) of this invention.

Particularly, Fig. 1 to Fig. 9 are views concerning the manufacture of a polycrystalline semiconductor thin film substrate and Fig. 10 and Fig. 11 are views illustrating a method of manufacturing a thin film transistor by using the polycrystalline semiconductor thin film substrate.

Fig. 2(a) - (d) illustrate a method (process) of forming a polycrystalline semiconductor thin film of this Embodiment 1.

At first as shown in Fig. 2(a), an insulative substrate 602 (for example, glass, fused quartz, sapphire, plastic and polyimide) is placed on a heating plate 606 (for example, carbon resistance heating heater). Subsequently, an amorphous semiconductor film 601 (for example, Si, Ge and SiGe) is deposited on the insulative substrate 602 by using a chemical vapor phase deposition method or a sputter deposition method on the insulative substrate 602. The thickness of the amorphous semiconductor film 601 is preferably 60 nm or less.

Then, as shown in Fig. 2(b), the heating plate 606 is heated to a predetermined temperature of 100°C or higher. In this case, a care should be taken so as not to cause unevenness in the temperature for the insulative substrate 602 and the amorphous semiconductor film 601.

Then, the surface of the amorphous semiconductor film 601 is scanned by a first laser irradiation (first excimer laser irradiation) 604 (for example, KrF or XeCl) in the direction of an arrow 603. The first excimer laser irradiation 604 is

applied repeatedly for multiple times at a suitable shape selection laser energy density  $E_c$  ( $360 \text{ mJ/cm}^2$ ), which is to be set as described later. Further, after the first excimer laser irradiation 604, second laser irradiation (second excimer laser irradiation) 605 is applied at a laser energy density lower than the suitable shape selection laser energy density  $E_c$  (for example,  $320 \text{ mJ/cm}^2$ ). For example, each of the first excimer laser irradiation 604 and the second excimer laser irradiation 605 is applied by the number of 30 to 60 cycles.

Now, the suitable shape selection laser energy density  $E_c$  set by the present inventors and the polycrystalline semiconductor thin film formed by the laser beam irradiation are to be explained.

Fig. 6 is a group of graphs showing the result of analysis such as for the properties of the crystal grains and the difference of the manufacturing conditions in the manufacture of a polycrystalline semiconductor thin film, in which Fig. 6(a) is a graph showing a correlation between the shape (N) and the number density of crystal grains, Fig. 6(b) is a graph showing a correlation between (N) and the full width at half maximum and Fig. 6(c) is a graph showing a correlation between the laser energy density and the formed shape (N).

Fig. 7 is a graph showing a correlation between hexagonal crystal grains and the number of laser beam irradiation cycles, and a graph showing a relation between the

number of laser beam irradiation cycles and the roughness on the surface of the polycrystalline semiconductor thin film in the manufacture of the polycrystalline semiconductor thin film. Examples of crystal grains according to the existent method of manufacturing a polycrystalline semiconductor thin film by crystallizing an amorphous semiconductor film by laser heating includes trigonal, tetragonal, pentagonal, hexagonal, heptagonal and octagonal shapes as described above. Their distribution is as shown in Fig. 6(a). In the graph  $N$  is taken on the abscissa and the number density is taken on the ordinate.

$N$  is a number of closest crystal grains for an optional crystal grain. When the statistical distribution is examined for  $N$ , it forms a normal distribution as shown in Fig. 6(a). The full width at half maximum of the normal distribution corresponds to the uniformness of the polycrystalline film in which the polycrystalline film is made more uniform as the full width at half maximum is narrower.

Fig. 6(b) shows a relation between the full width at half maximum and  $N$ . The full width at half maximum takes a minimum value at  $N = 6$ .  $N = 6$  is equivalent with that the surface shape of the crystal grains (the optional crystal grain) is hexagonal.

Fig. 6(c) illustrates a relation between the laser energy density and  $N$  when the amorphous semiconductor film is laser heated at  $100^{\circ}\text{C}$  or higher.  $N$  is 6 when the energy density

is  $E_c$ . That is, it has been found that the crystal grains tend to form hexagonal crystal grains when the laser energy density is  $E_c$ . Then,  $E_c$  is defined as the suitable shape selection laser energy density  $E_c$ .

Fig. 7(a) illustrates that the optimum number of laser irradiation cycles  $M$  is  $M_c$  when laser beam irradiation is applied at the laser energy density of  $E_c$  or lower at a temperature of the amorphous semiconductor film of  $100^\circ\text{C}$  or higher.

Fig. 7(b) illustrates a relation between the number of laser beam irradiation cycles  $M$  and the roughness on the surface of the polycrystalline semiconductor thin film in a case where the laser irradiation (second laser irradiation) is applied at a laser energy density of  $E_c$  or lower at a temperature of the amorphous semiconductor film of  $100^\circ\text{C}$  or higher. The roughness is defined as a top-to-bottom maximum length. Specifically, the top-to-bottom length at the corner of the grain boundary corresponds to this. Along with increase in  $M$ , the roughness decreases to 5 nm or less. Further, chemical bonds in the grain boundaries are bonded again.

Fig. 8(a) - (c) is a view illustrating the difference in the shape of crystal grains in the polycrystalline semiconductor film due to the difference of the laser beam density. The view is obtained based on microscopic photography.

Fig. 8 (a) illustrates the state of crystal grains in

the polycrystalline semiconductor film at a laser energy density lower than the suitable shape selection laser energy density  $E_c$ . As can be seen from the figure, while crystal grains contain many hexagonal shapes, trigonal, tetragonal or pentagonal shapes are also present. The hexagonal crystal grains are about 30 to 40% or less.

Fig. 8 (b) is an example of forming a polycrystalline semiconductor thin film while applying laser beam irradiation repeatedly at a suitable shape selection laser energy density  $E_c$ . This is an example of applying the first laser irradiation at the suitable shape selection laser energy density  $E_c$  by multiple cycles and then applying the second laser irradiation at a laser energy density lower than the suitable shape selection laser energy density  $E_c$  repeatedly. For example, the laser energy density in the first laser irradiation is  $360 \text{ mJ/cm}^2$  (suitable shape selection laser energy density  $E_c$ ) and the laser energy density of the second laser irradiation is  $320 \text{ mJ/cm}^2$ . In this example, the hexagonal crystal grains can be formed by about 50 to 100% by increasing the number of cycles of repeating irradiation. Further, the hexagonal crystal grains are made uniform with a diameter of about  $0.2$  to  $0.3 \text{ }\mu\text{m}$ .

It was confirmed that 50 to 100% of the surface shape in the crystal grains constituting the polycrystalline semiconductor thin film is hexagonal, for example, by scanning

electron microscopic observation while taking a square evaluation region of  $10\text{ }\mu\text{m}$  size on one side including the center of the polycrystalline semiconductor thin film. The result of the observation for the evaluation region reflects the state of the crystal grains for the entire surface of the polycrystalline semiconductor thin film.

In the first laser irradiation, when laser beam irradiation is applied repeatedly by once or predetermined number of cycles, hexagonal crystal grains are formed successively as crystal grains and, subsequently, they continue to rotate or move as shown in Fig. 9(a) and then respective sides of adjacent hexagonal crystal grains meet each other as shown in Fig. 9(b). Further, according to the laser beam irradiation, impurities less segregate to the boundaries of the crystal grain and the carrier concentration of each of the crystal grains becomes constant.

As shown in Fig. 9(a), even when smaller crystal grain 1001 is formed between the hexagonal crystal grains 251, it is joined with large hexagonal crystal grains 251 at the periphery and eliminated in the step of the first laser irradiation and the step of the second irradiation applied repeatedly.

Further, in the second laser irradiation step, laser beam irradiation may be applied successively at the suitable shape selection laser energy density  $E_c$ .



Fig. 8(c) is an example of applying the laser beam irradiation at a laser energy density higher than the suitable shape selection laser energy density  $E_c$  in which remelting of crystals occurs and grain boundaries are re-bonded into large crystal grains in an island shape.

After the first laser beam irradiation, undulations 610 are formed on the surface of the polycrystalline semiconductor thin film 640 to form grain boundaries 611. The grain boundaries 611 include dangling bonds. Further, as shown in Fig. 2(b) - (d), the grain boundaries are gradually narrowed as 611, 621 and 631 and the surface roughness is also planarized successively as 610, 620 and 630 along with increase in the number of cycles of the laser beam irradiation.

By the method as described above, a polycrystalline semiconductor thin film substrate 260 as shown in Fig. 3 can be manufactured. Fig. 4 is a cross sectional view showing a portion of a polycrystalline semiconductor thin film substrate 260.

As can be seen also from the figure, a polycrystalline semiconductor thin film 640 with a planar surface is formed. Further, most of crystal grains in the polycrystalline semiconductor thin film 640 are also hexagonal crystal grains 251 as shown in Fig. 5. The hexagonal crystal grains 251 can be 50 to 100% depending on the manufacturing method.

The excimer laser irradiation is to be explained with

reference to Fig. 1. An excimer laser apparatus has an UV-lamp heating device 106 at a lower portion and has an excimer laser (excimer laser generator) 101 at a corresponding upper portion. The UV-lamp heating device 106 and the excimer laser 101 are controlled by a control device 107.

An insulative substrate (glass substrate) 602 having an amorphous semiconductor film (amorphous silicon film) 601 at the upper surface is disposed on the UV lamp heating device 106 and preliminarily heated by the UV lamp heating device 106. Further, a laser beam (excimer laser beam) 660 is irradiated from the excimer laser 101. Since a not illustrated stage for supporting the insulative substrate 602 is moved relatively to the excimer laser 101, the excimer laser beam 660 can be irradiated to the entire region of the amorphous semiconductor film 601 on the upper surface of the insulative substrate 602 to be formed into a polycrystalline semiconductor thin film.

In this Embodiment 1, the laser beam irradiation is applied for two steps of the first excimer laser irradiation 604 and the second excimer laser irradiation 605. In each of the steps, the laser beam irradiation is applied repeatedly for about 30 to 60 cycles. Further, the laser beam irradiation is applied in the first excimer laser irradiation 604 at the suitable shape selection laser energy density  $E_c$  and the laser beam irradiation is applied in the second excimer laser irradiation 605 at a laser energy density lower

than the suitable shape selection laser energy density  $E_c$ . In the second excimer laser irradiation 605, it may be applied at a constant laser energy density, or the laser beam irradiation may be applied while lowering the laser energy density gradually in the course of irradiation.

According to the method of manufacturing the polycrystalline semiconductor thin film substrate of this Embodiment 1, 50 to 100% of the crystal grains 250 of the polycrystalline semiconductor thin film 640 comprise hexagonal crystal grains 251 and the grain size is uniform as 0.2 to 0.3  $\mu\text{m}$ , so that it is possible to provide a polycrystalline semiconductor thin film substrate with an improved carrier mobility  $\mu$  and with less variation in the carrier mobility  $\mu$  in each of the regions. The carrier mobility  $\mu$  can be enhanced, for example, to about 200 - 300  $\text{cm}^2/\text{V}\cdot\text{s}$ .

Further, since electron orbits in the grain boundaries on the surface and inside the polycrystalline semiconductor thin film are bonded, it can provide an effect of making the carrier mobility constant and improving the reliability of individual transistors.

Further, when the polycrystalline semiconductor thin film 640 is formed, since the laser beam is irradiated repeatedly, the roughness on the surface of the polycrystalline semiconductor thin film 640 is reduced and a planar polycrystalline semiconductor thin film substrate can

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be provided. For example, the roughness can be restricted to 5 nm or less.

Further, when the polycrystalline semiconductor thin film 640 is formed, since the laser beam irradiation is applied repeatedly for multiple cycles at the suitable shape selection laser energy density  $E_c$  most preferred for forming the hexagonal shape, hexagonal seed crystals are successively formed in the amorphous semiconductor film and adjacent hexagonal crystal grains move to each other and are successively in close contact with adjacent hexagonal crystal grains 251. Subsequently, since the laser beam irradiation is applied repeatedly for multiple cycles at a laser energy density lower than the suitable shape selection laser energy density  $E_c$ , impurities less segregate to the grain boundary and the carrier concentration is made constant for each of the crystal grains.

The atmosphere upon UV-lamp heating and laser heating in this embodiment may be vacuum, inert gas (for example, argon, krypton or helium) or nitrogen gas.

Then, a method of manufacturing a thin film transistor is to be explained. For example, as shown in Fig. 11(a), an insulative substrate (glass substrate) 602 having a polycrystalline semiconductor thin film (polycrystalline silicon film) 640 at the surface is provided. The example of Fig. 11 has a structure in which a silicon oxide film 651 is

placed as a buffer layer between the insulative substrate 602 and the polycrystalline semiconductor thin film 640, different from the polycrystalline semiconductor thin film substrate 260 shown in Fig. 3. While the buffer layer may be saved, this Embodiment 1 is to be explained for the method of manufacturing a thin film transistor in a polycrystalline semiconductor thin film substrate 260 having the buffer layer.

As shown in Fig. 11(a), a photoresist film 670 is disposed selectively for forming a channel region 672 of the transistor and, subsequently, phosphorus (P) is implanted into the polycrystalline semiconductor thin film 640 and annealing is applied to form an n-type impurity region 671. The impurity region 671 forms a source region or a drain region. If necessary, predetermined impurities are doped to the polycrystalline semiconductor thin film 640 in the step of forming the polycrystalline semiconductor thin film.

Then, as shown in Fig. 11(b), selective etching is applied to extend impurity regions 671 each of a predetermined length on both sides of the channel regions 672.

Then, as shown in Fig. 11(b), a silicon oxide film is formed over the entire region on the upper surface of the insulative substrate 602 to form a gate insulation film 673.

Then, as shown in Fig. 11(b), a gate 674 is formed above the channel region 672.

Alternatively, the impurity regions 671 to form the

source region and the drain region may be formed by disposing a gate insulation film 673 and forming a gate electrode 674 and then implanting phosphorus into the polycrystalline semiconductor thin film 640 using the gate electrode 674 as a mask without conducting the impurity diffusion as described above.

Then, after forming an interlayer insulation film 675 over the entire region of the upper surface of the insulative substrate 602, contact holes are opened to form electrodes (source electrode, drain electrode) 676 to be connected with the impurity region 671 or not illustrated gate wiring electrode. Further, although not illustrated, the transistor is covered with a passivation film and a portion of the passivation film is removed to expose an external electrode.

While only one transistor is illustrated in the figure, it is actually formed in plurality.

In the transistor according to this Embodiment 1, since 50% to 100% of the crystal grains of the polycrystalline semiconductor thin film 640 comprise hexagonal crystal grains 251 and the grain diameter is uniform as 0.2 to 0.3  $\mu\text{m}$ . Accordingly, when a transistor (TFT) is formed, the grain boundaries in the channel region of silicon below the gate electrode are reduced and the carrier mobility  $\mu$  is improved and variation in the carrier mobility is decreased for each of the transistors. The carrier mobility  $\mu$  can be enhanced, for

example, to about 200 - 300 cm<sup>2</sup>/V's.

Further, the variation in the density of the grain boundaries present in the channel region of silicon below the gate electrode is reduced in each of the transistors, and the threshold voltage  $V_{th}$  is made uniform for each of the transistors. Variation in the threshold voltage  $V_{th}$  can be suppressed to 0.1 V or lower.

Further, since the laser beam is irradiated repeatedly when the polycrystalline semiconductor thin film 640 is formed, the roughness on the surface of the polycrystalline semiconductor thin film is reduced, and variation in the performance is decreased for each of the individual transistors and degradation less occurs to attain longer life of the transistor.

Further, when the polycrystalline semiconductor thin film 640 is formed, since the laser beam irradiation is applied repeatedly by multiple cycles at a suitable shape selection laser energy density  $E_c$  for forming the hexagonal shape, hexagonal seed crystals are formed successively and adjacent hexagonal crystal grains move to each other and are in close contact with adjacent hexagonal crystal grains successively. Subsequently, laser beam irradiation is applied repeatedly for multiple cycles at a laser energy density lower than the suitable shape selection laser energy density  $E_c$ . Accordingly, impurities less segregate in the grain boundaries

and the carrier concentration are made constant for each of the crystal grains. As a result, characteristics of the transistor become stable.

Further, since crystal grains of uniform shape and size are formed in the transistor channel region and chemical bonds of the grain boundaries are re-bonded to provide a surface with less roughness, the interface density of state between the semiconductor and the gate insulation film can be lowered to lower the threshold voltage  $V_{th}$ . Further, by the same reasons as described above, variation due to short-channel can be suppressed.

In this embodiment, since the crystal grains in the polycrystalline semiconductor thin film are formed as the hexagonal crystal grains of uniform size, the carrier mobility is high and it less varies, as well as the threshold voltage  $V_{th}$  less varies. Accordingly, when plural transistors are manufactured, characteristics less scatter for each of the transistors and the manufacturing yield of semiconductor devices can be improved. As a result, the manufacturing cost of the semiconductor device can be reduced.

#### Embodiment 2

Fig. 12 is a schematic view illustrating the state of forming a polycrystalline semiconductor thin film as another embodiment (Embodiment 2) of this invention.



In the excimer laser device of Embodiment 2, as shown in Fig. 12, an insulative substrate (glass substrate) 602 having an amorphous semiconductor film (amorphous silicon film) 601 at the upper surface is located between a UV-lamp heating device 106 in the lower portion and an excimer laser (excimer laser generator) 101 in the upper portion, and the UV-lamp heating device 106 and the excimer laser 101 are controlled by the control device 107. Preliminary heating is applied by the UV-lamp heating device 106 and the amorphous semiconductor film 601 is formed into a polycrystalline semiconductor thin film by a laser beam 160 emitted from the excimer laser 101.

In Embodiment 2, the UV-lamp heating device 106 and the excimer laser 101 are controlled by using the control device 107 to synchronize the light emitting interval of the UV-rays and the excimer laser irradiation. In this case, thermally-induced strain formed between the insulative substrate 602 and the amorphous semiconductor film 601 can be controlled.

### Embodiment 3

Fig. 13 is a schematic view illustrating the state of forming a polycrystalline semiconductor thin film as another embodiment (Embodiment 3) of this invention. Explanation is to be made, particularly, for the constitution of the excimer

laser beam irradiation in Fig. 3.

A laser beam 110 emitted from an excimer laser 101 is irradiated to an amorphous semiconductor film 601 at the upper surface of an insulative substrate 602 placed on a sample stage 122. In this Embodiment 3, the laser beam 110 emitted from the excimer laser 101 splits in two optical channels by an optical component such that one of them reaches a laser beam irradiation position with a delay.

That is, the laser beam 110 emitted from the excimer laser 101 is divided by a half mirror 102 into two optical channels in which one of them passes through a mirror 103 and a mirror 105 and reaches a laser beam irradiation position, while the other is reflected at the half mirror 102 and then directly reaches the laser beam irradiation position.

With this constitution, a laser beam 112 passing through an optical channel of a shorter optical channel length can preliminarily heat the amorphous semiconductor film 601 and melts the amorphous semiconductor film 601 together with a laser beam 111 that reaches passing through an optical channel of a longer optical channel length with a delay.

Then, laser beam irradiation is applied repeatedly for multiple cycles at the suitable shape selection laser energy density  $E_c$  as the first laser irradiation step and, successively, the laser beam irradiation is applied repeatedly for multiple cycles at a laser energy density lower than the

suitable shape selection laser energy density  $E_c$  as the second laser irradiation step, thereby enabling to manufacture a polycrystalline semiconductor thin film substrate at a good quality in the same manner as in the previous embodiments.

#### Embodiment 4

In Embodiment 4, an electronic apparatus incorporated with a transistor (thin film transistor) manufactured by the previous embodiment will be described.

Fig. 14 is a schematic perspective view illustrating a portion of a liquid crystal display according to another embodiment (Embodiment 4) of the present invention.

Explanation is to be made in this Embodiment 4 to an example of incorporating a semiconductor device 40 formed with plural transistors (thin film transistors) 18 to a polycrystalline semiconductor thin film substrate 260 (amorphous semiconductor film 601 formed on the upper surface of the insulative substrate 602) into an image display apparatus (electronic apparatus).

Fig. 14 is a perspective view in an exploded state illustrating a portion of the image display apparatus. As shown in Fig. 14, it is constituted such that liquid crystals are disposed on a semiconductor device 40 in which a group of transistors are formed to the upper surface of a polycrystalline semiconductor thin film substrate 260 and a

display panel 22 constituting pixels 23 is stacked and glass-encapsulated. Transistors 18 as the pixel driver correspond to each of the pixels 23, and the source electrode of the transistor 18 and the pixel electrode of the pixel 23 are connected to each other by stacking.

Peripheral driver circuits 19 such as an address decoder, a digital/analog conversion circuit and a controller are disposed to the periphery out of the region in which the pixels 23 are arranged. Reference numerals 10 and 21 show transistor forming regions.

In the electronic apparatus described above, since the size of the crystal grains is uniform in the channel region of each of the transistors 18 corresponding to the pixel 23, the carrier mobility is constant and the threshold voltage  $V_{th}$  is also constant as described in Embodiment 1, image display at high performance is possible and reliability can be improved in an image display of a large area.

#### Embodiment 5

Fig. 15 is a schematic perspective view illustrating a portion of a data processor according to another embodiment (Embodiment 5) of this invention and Fig. 16 is an enlarged schematic view of a portion surrounded with a dotted chain circle in Fig 16.

Also in this Embodiment 5, crystal grains to be used

are formed on the surface of an insulative substrate 602, that is, a glass substrate to form a polycrystalline semiconductor thin film substrate 260 by the same method as in Embodiment 1.

A data processor 30 comprises each of circuitries formed on the surface of a polycrystalline semiconductor thin film substrate 260. That is, as shown in Fig. 15, transistors 18 and passive elements not shown are formed on the surface of the polycrystalline semiconductor thin film substrate 260. Further, each of the circuitries is connected with wirings not shown and has such a structure in which external terminals are disposed on the surface of the polycrystalline semiconductor thin film substrate 260 or connectors are attached to the edges thereof.

Further, each of the circuit portions and wirings on the surface of the polycrystalline semiconductor thin film substrate are covered and protected with a passivation film. Reference numeral 10 denotes a transistor film region.

The data processor 30 comprises, for example, a central processing unit 24, a memory circuitry 26, an input/output controller 28 and a peripheral circuitry 27 connected respectively by way of a data bus circuitry 29 to the central processing unit 24, and a cash circuitry 25 connected with the central processing unit 24.

In the data processor 30, each of the transistors is formed into a polycrystalline semiconductor thin film. Since

each of the transistors is formed as a polycrystalline semiconductor thin film with the uniform size of the crystal grains and with uniform grain boundaries in the channel region, the carrier mobility  $\mu$  is high with less variation and also the variation in the threshold voltage  $V_{th}$  is small.

Accordingly, the electric field effect mobility is higher than that formed in the existent polycrystal semiconductor thin film and the manufacturing cost of the data processor 30 can also be reduced.

The inventions made by the present inventors have been explained concretely with reference to the preferred embodiments but it will be apparent that the inventions are not limited to the embodiments described above and can be modified variously within a scope not departing the gist thereof.

Further, in the foregoing explanations, although the inventions made by the present inventors have been described in the case where the invention is applied to the image display or the data processor in the field of use as the background of the invention, it is not limited thereto and is applicable also to other electronic devices.

These inventions are applicable at least to electronic devices that can be manufactured by using the polycrystalline semiconductor thin film.

The effects obtainable by typical inventions among those disclosed in the present application will be simply explained as

below.

(1) In the polycrystalline semiconductor thin film substrate, the crystal grains of the polycrystalline semiconductor thin film can be formed into the hexagonal crystal grains of a uniform size and the ratio of the hexagonal crystal grains can be 50 to 100%.

(2) In the polycrystalline semiconductor thin film substrate, it is possible to provide the polycrystalline semiconductor thin film substrate in which the size and the carrier concentration are uniform and the surface is planar.

(3) A semiconductor device having the thin film transistor of favorable characteristics and with less variation in characteristics can be provided.

(4) A semiconductor device having the thin film transistor of high carrier mobility and with less variation in characteristics can be provided.

(5) The yield of the semiconductor devices can be enhanced and reduction in the manufacturing cost for the semiconductor device can be attained.

(6) Electronic apparatus such as a liquid crystal display and a data processing unit at favorable high speed performance can be provided.

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CLAIMS

1. A polycrystalline semiconductor thin film substrate comprising an insulative substrate and a polycrystalline semiconductor thin film formed on one surface of the insulative substrate, wherein in which the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film.

2. A polycrystalline semiconductor thin film substrate as defined in claim 1, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

3. A semiconductor device comprising plural transistors formed in a polycrystalline semiconductor thin film, wherein the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film.

4. A semiconductor device as defined in claim 3, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

5. A semiconductor device comprising plural transistors formed in a polycrystalline semiconductor thin film, wherein a square region with a 10  $\mu$  side and in which 50 to 100% of the crystal grains have the number of closest crystalline grains of



6 is present so as to include the center of the polycrystalline semiconductor thin film in the polycrystalline semiconductor thin film.

6. A semiconductor device as defined in claim 5, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

7. An electronic apparatus comprising a semiconductor device in which plural transistors are formed in a polycrystalline semiconductor thin film, wherein variation in the threshold voltage of the plural transistors is 0.1 V or less.

8. An electronic apparatus as defined in claim 7, wherein the number of crystal grains with the number of closest crystal grain of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film.

9. An electronic apparatus as defined in claim 8, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

10. An electronic apparatus comprising a semiconductor device in which plural transistors are formed in a polycrystalline semiconductor thin film wherein a square region with a 10  $\mu\text{m}$  side and 50 to 100% of the crystal grains have the number of closest crystalline grains of 6 is present so as to include the center of the polycrystalline semiconductor thin film in the polycrystalline semiconductor thin film.

11. An electronic apparatus as defined in claim 10,

wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

12. An electronic apparatus as defined in claim 7, wherein the electronic apparatus is a liquid crystal display, the semiconductor device has transistors for operating each of pixels of a liquid crystal display panel and transistors constituting peripheral driver circuitries and is stacked and attached on the liquid crystal display panel of the liquid crystal display.

13. An electronic apparatus as defined in claim 7, wherein the electronic device is a data processor, and a central processing unit, a cash circuitry, a memory circuitry, a peripheral circuitry, an input/output circuitry and a bus circuitry are formed with each of the transistors of the semiconductor device.

14. A method of manufacturing a polycrystalline semiconductor thin film substrate by forming an amorphous semiconductor thin film on the surface of an insulative substrate, then irradiating the amorphous semiconductor film with a laser beam thereby to crystallize the amorphous semiconductor film and forming a polycrystalline semiconductor thin film, wherein the method comprises irradiating the rear face of the insulative substrate or the amorphous semiconductor film with a UV-ray thereby to heat the amorphous semiconductor film to a melting temperature or lower, and repeatedly

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irradiating the surface of the amorphous semiconductor film with a laser beam at a suitable shape selection laser energy density  $E_c$  to form greatest number of crystal grains with the number of closest crystal grains of 6, synchronizing the period of the laser beam irradiation and the period of the UV-ray heating, and dividing, by an optical component, the laser beam into two optical channels with the optical length of one of them being made longer such that it reaches the laser beam irradiation position with a delay, thereby forming the polycrystalline semiconductor thin film.

15. A method of manufacturing a polycrystalline semiconductor thin film substrate as defined in claim 14, wherein one of the laser beams divided into two optical channels that passes through a channel of a shorter optical wavelength is attenuated by being passed through an optical attenuator and caused to reach the laser beam irradiation position, thereby forming the polycrystalline semiconductor thin film.

16. A semiconductor device in which a transistor is formed in a polycrystalline semiconductor thin film wherein the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains forming the channel region of the transistor.

17. A semiconductor device in which plural transistors are formed in the polycrystalline semiconductor thin film wherein a square region with a 10  $\mu\text{m}$  side and in which 50 to

100% of the crystal grains have the number of closest crystalline grains of 6 is present so as to include the center of the polycrystalline semiconductor thin film in the polycrystalline semiconductor thin film.

18. A semiconductor device as defined in claim 17, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

19. An electronic apparatus having plural transistors formed in a polycrystalline semiconductor thin film, wherein the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains forming the polycrystalline semiconductor thin film.

20. An electronic apparatus as defined in claim 19, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less.

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## ABSTRACT

A method of manufacturing a semiconductor device of forming an amorphous semiconductor film on the surface of an insulative substrate, then irradiating the amorphous semiconductor film with a laser beam to crystallize the amorphous semiconductor film thereby to form a polycrystalline semiconductor thin film, and then forming a transistor in the polycrystalline semiconductor thin film, wherein a UV-ray is irradiated to the rear face of the insulative substrate or the amorphous semiconductor film to heat the amorphous semiconductor film to a melting temperature or lower, and a laser beam at a suitable shape selection laser energy density  $E_c$  to form the crystal grains with the number of closest crystal grains of 6 most predominantly is irradiated to the surface of the amorphous semiconductor film to convert it into a polycrystalline semiconductor thin film, and then a transistor is formed in the polycrystalline semiconductor thin film.

A thin film transistor at high yield and having a high-speed operation can be manufactured.

FIG. 1

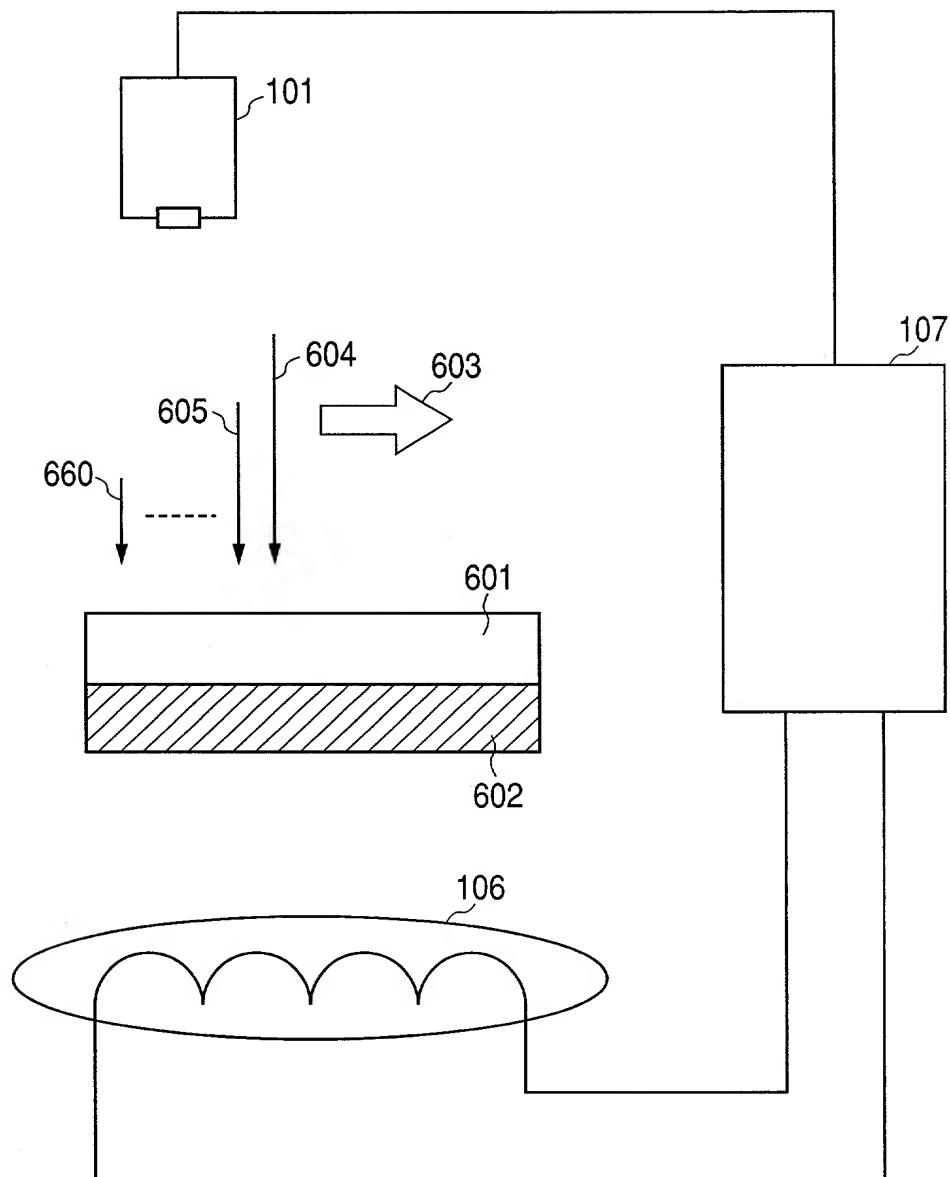


FIG. 2

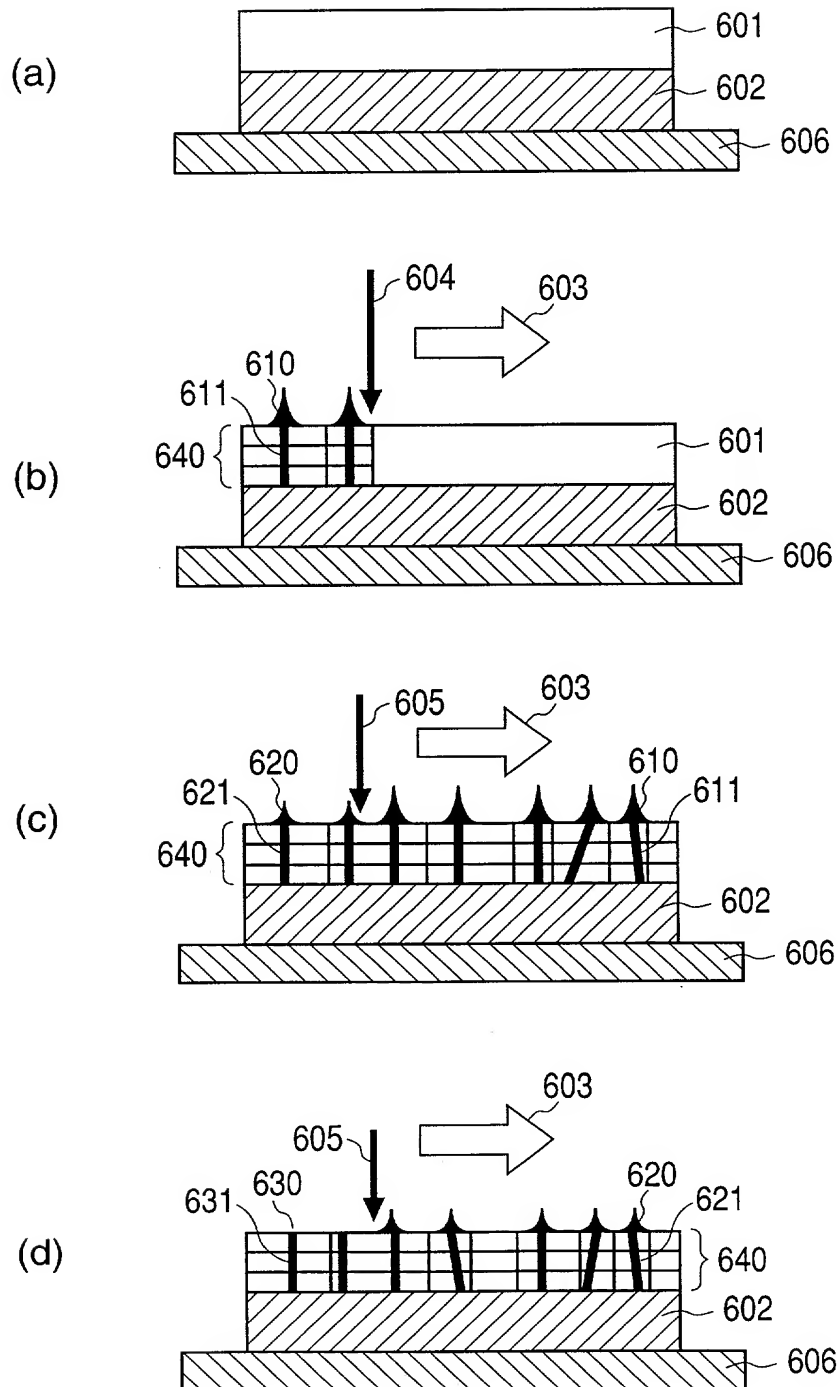


FIG. 3

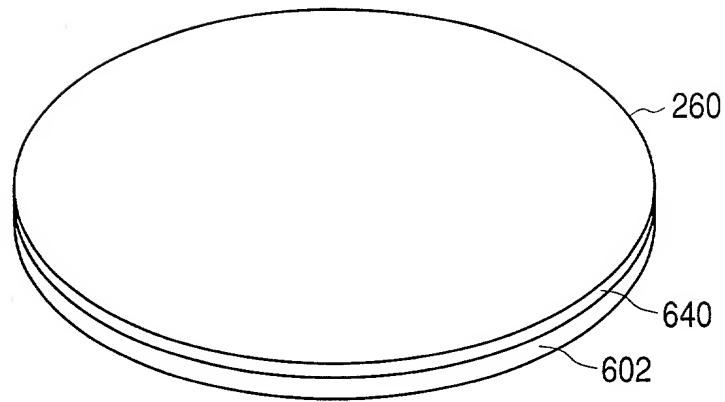


FIG. 4

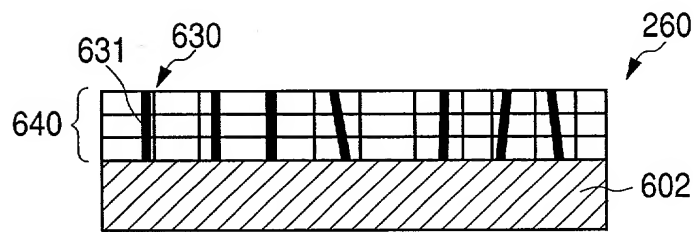
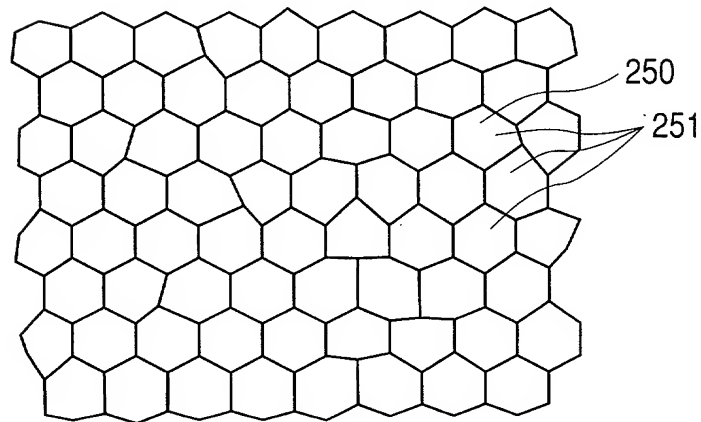
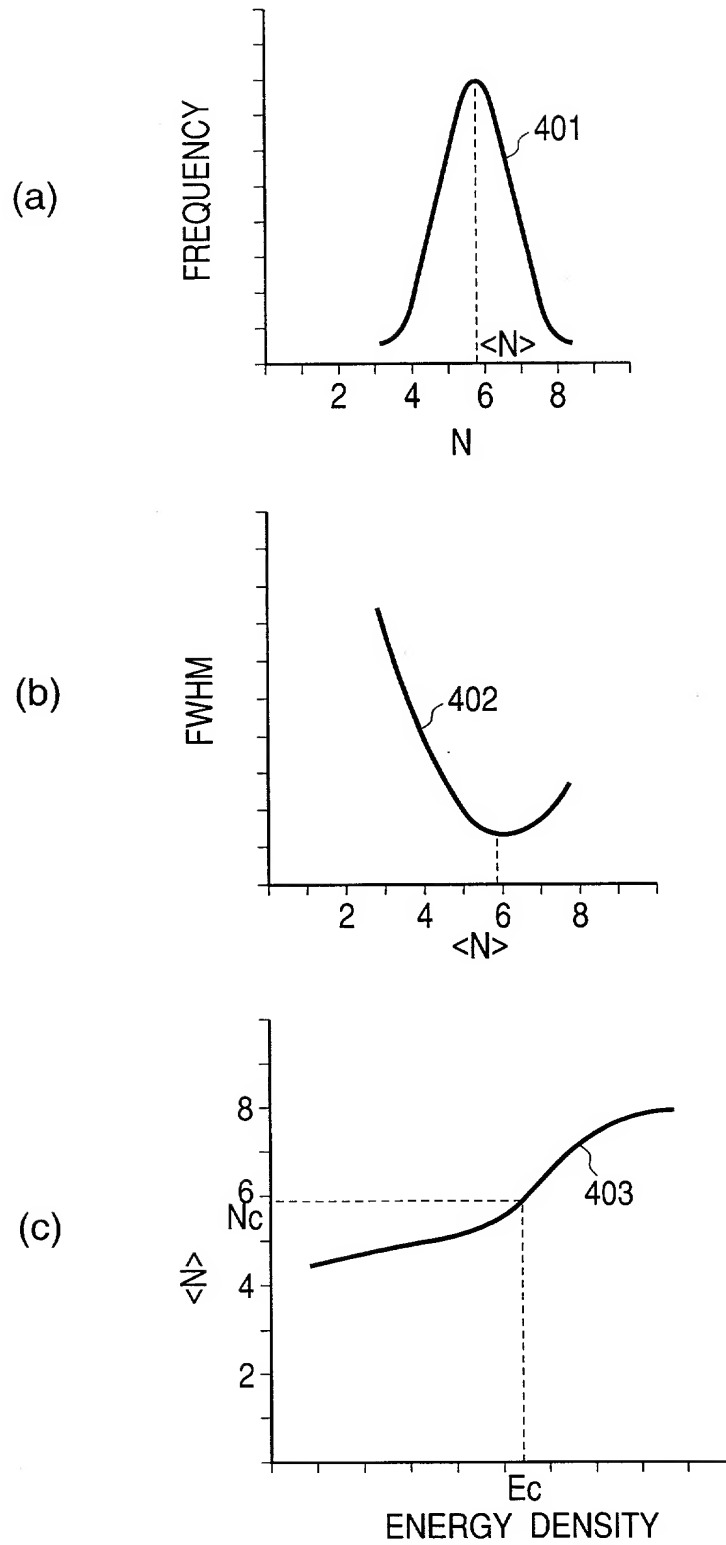


FIG. 5



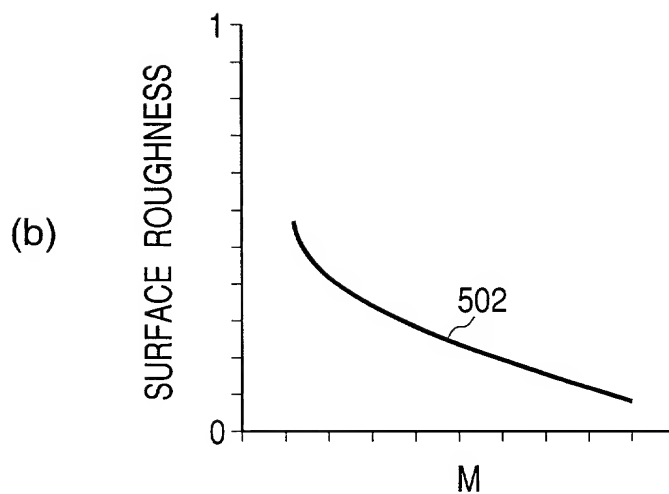
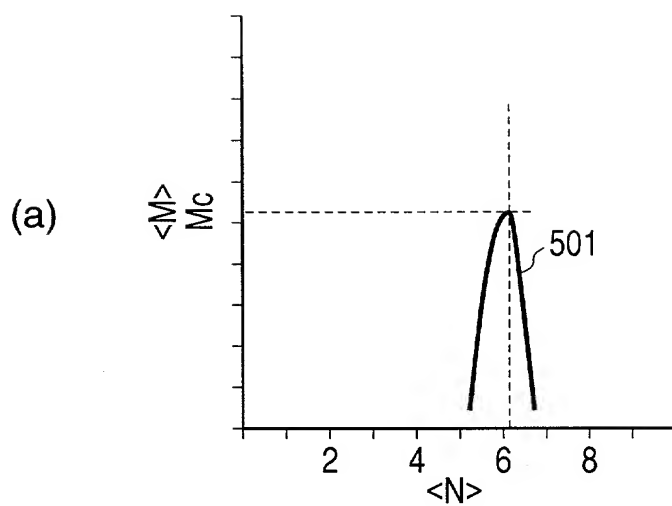


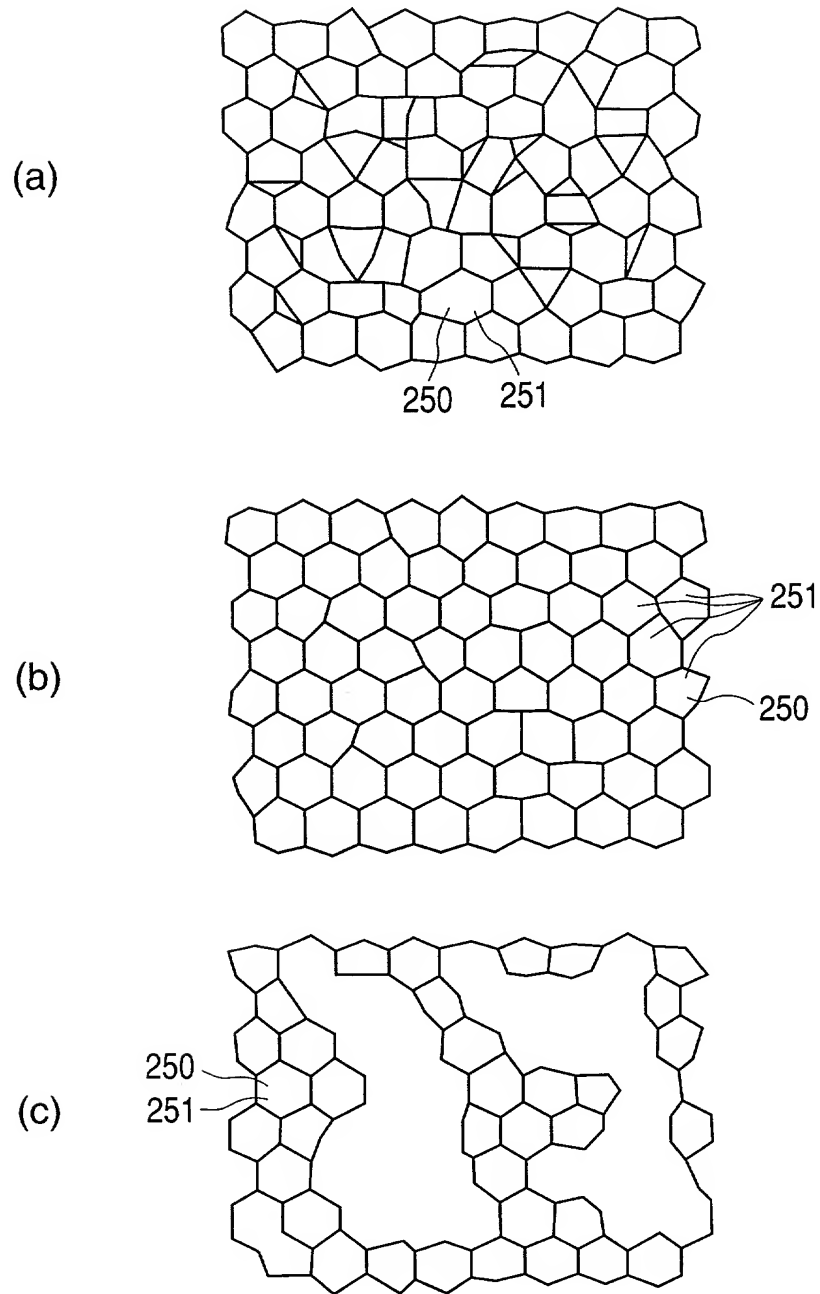
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**FIG. 6**

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FIG. 7

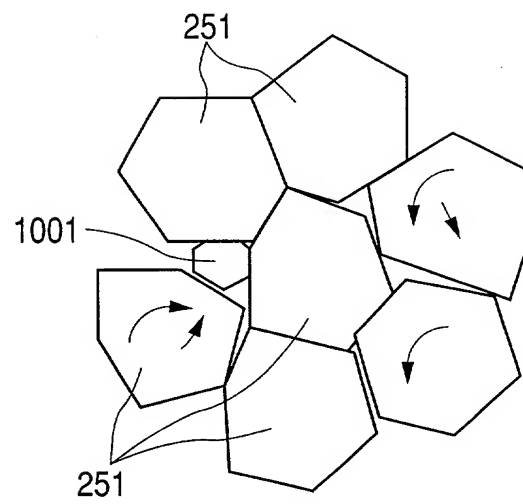


**FIG. 8**

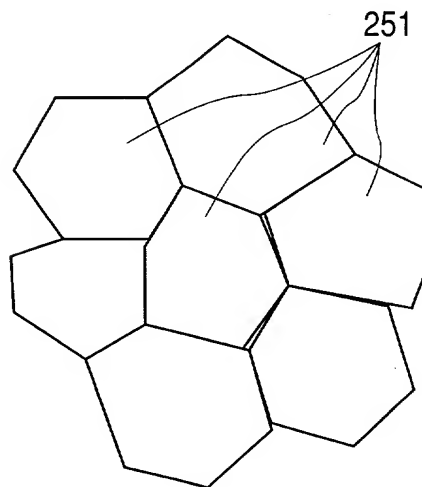
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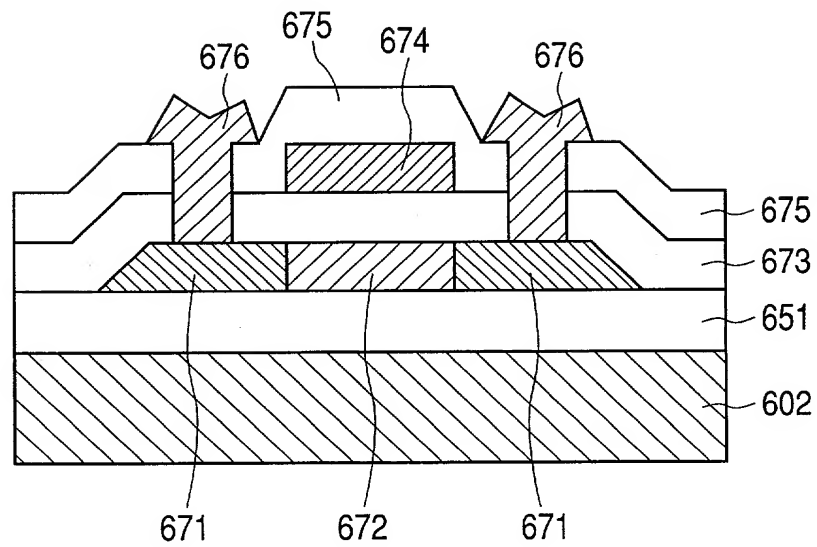
**FIG. 9**

(a)

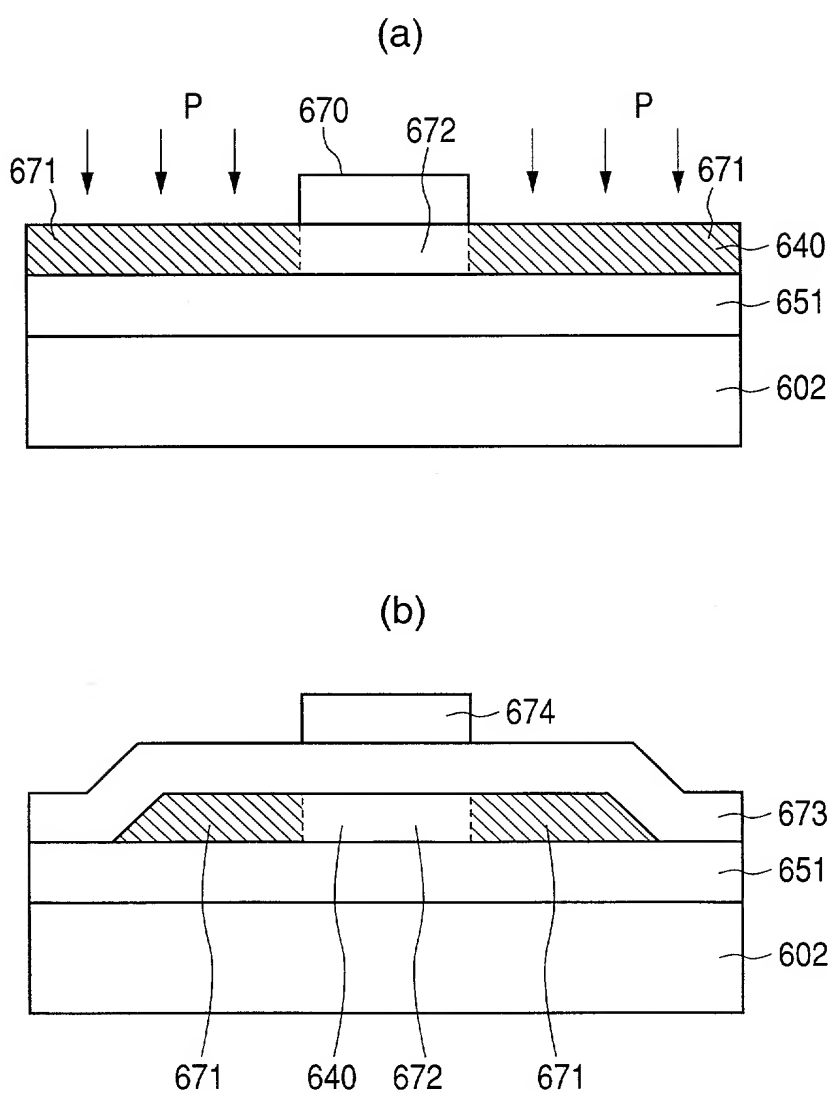


(b)



*FIG. 10*

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**FIG. 11**

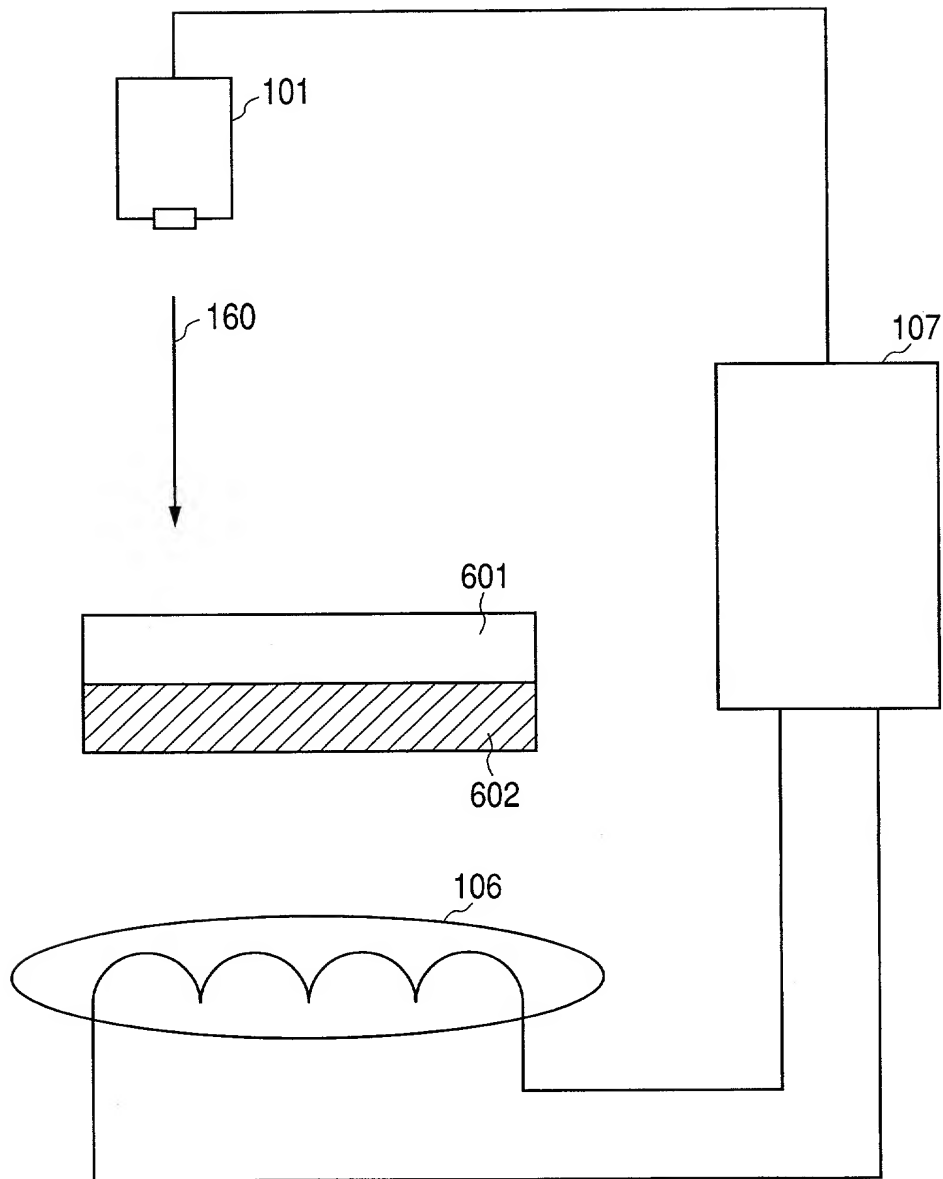
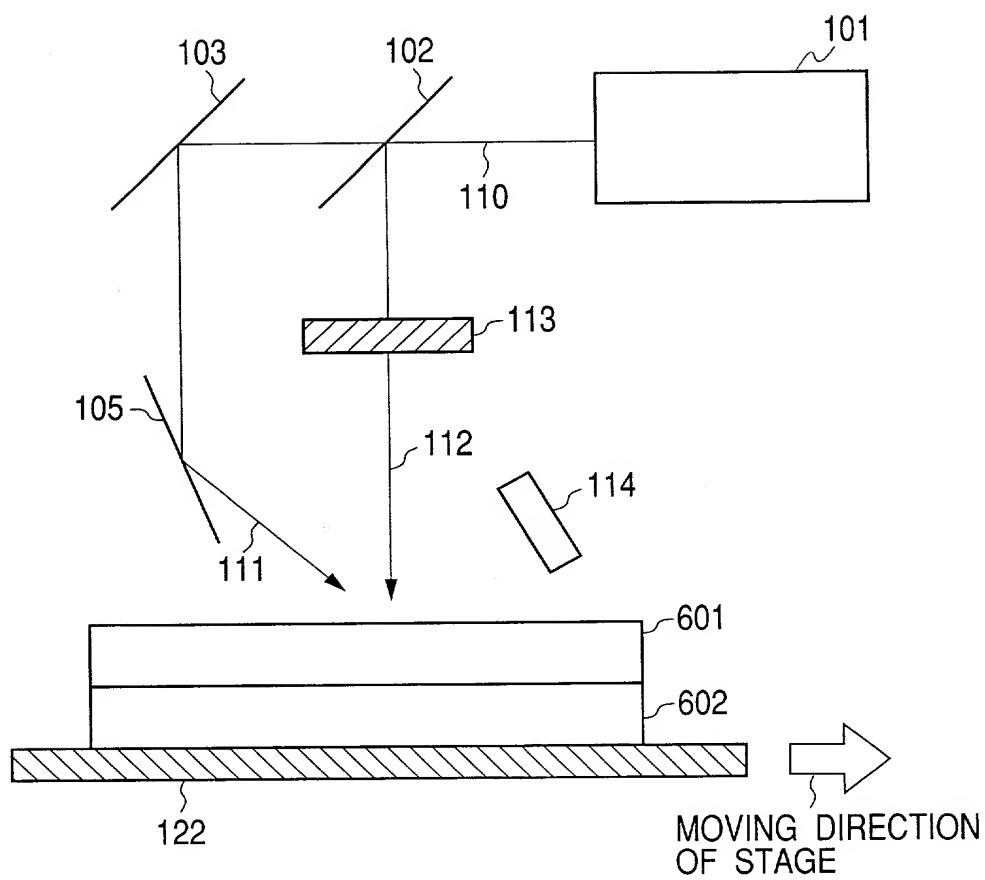
*FIG. 12*

FIG. 13





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FIG. 14

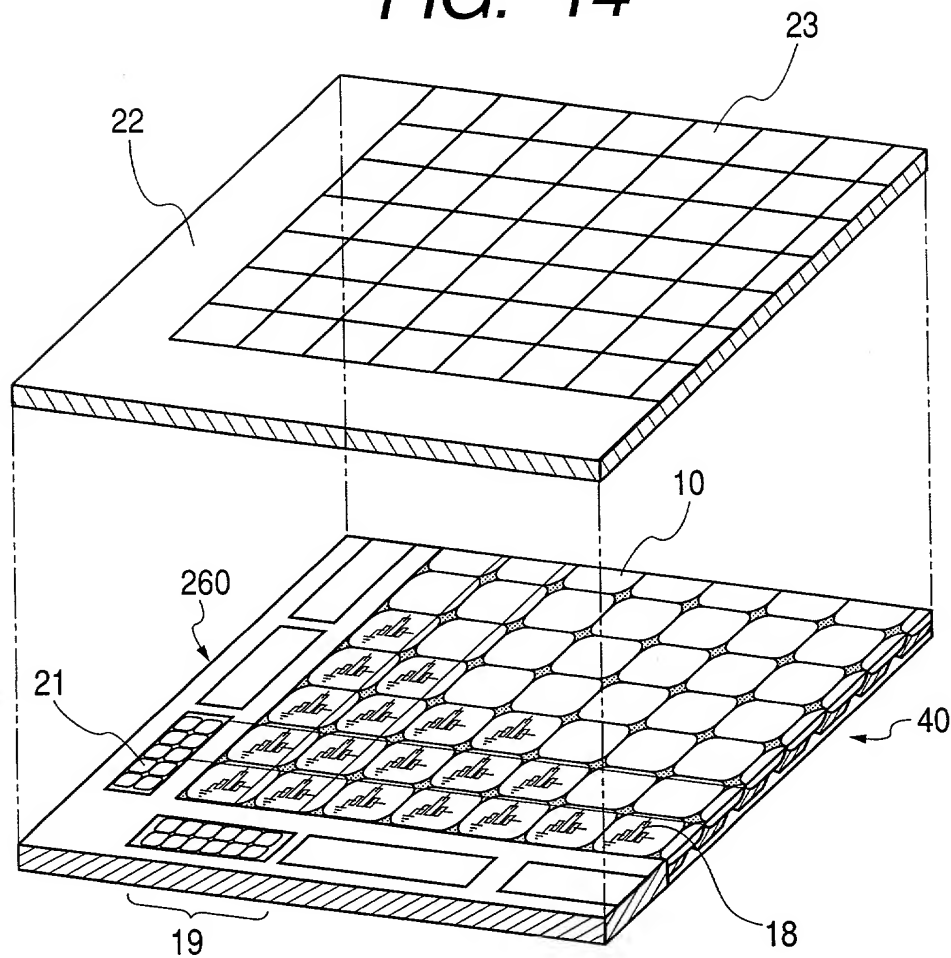


FIG. 15

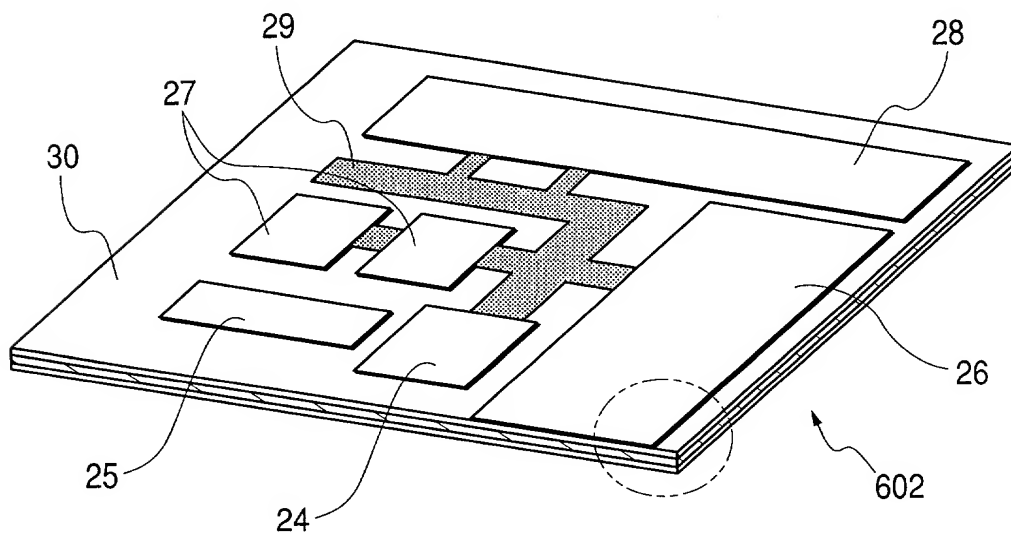
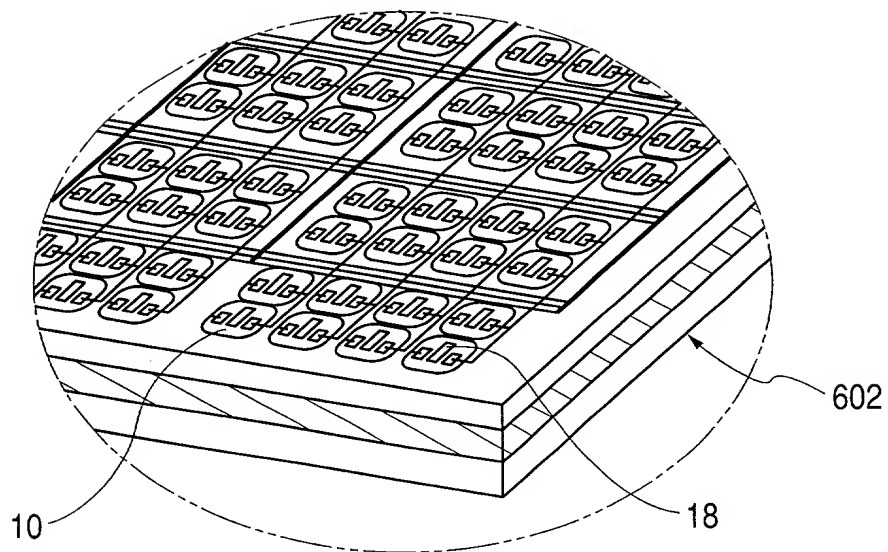
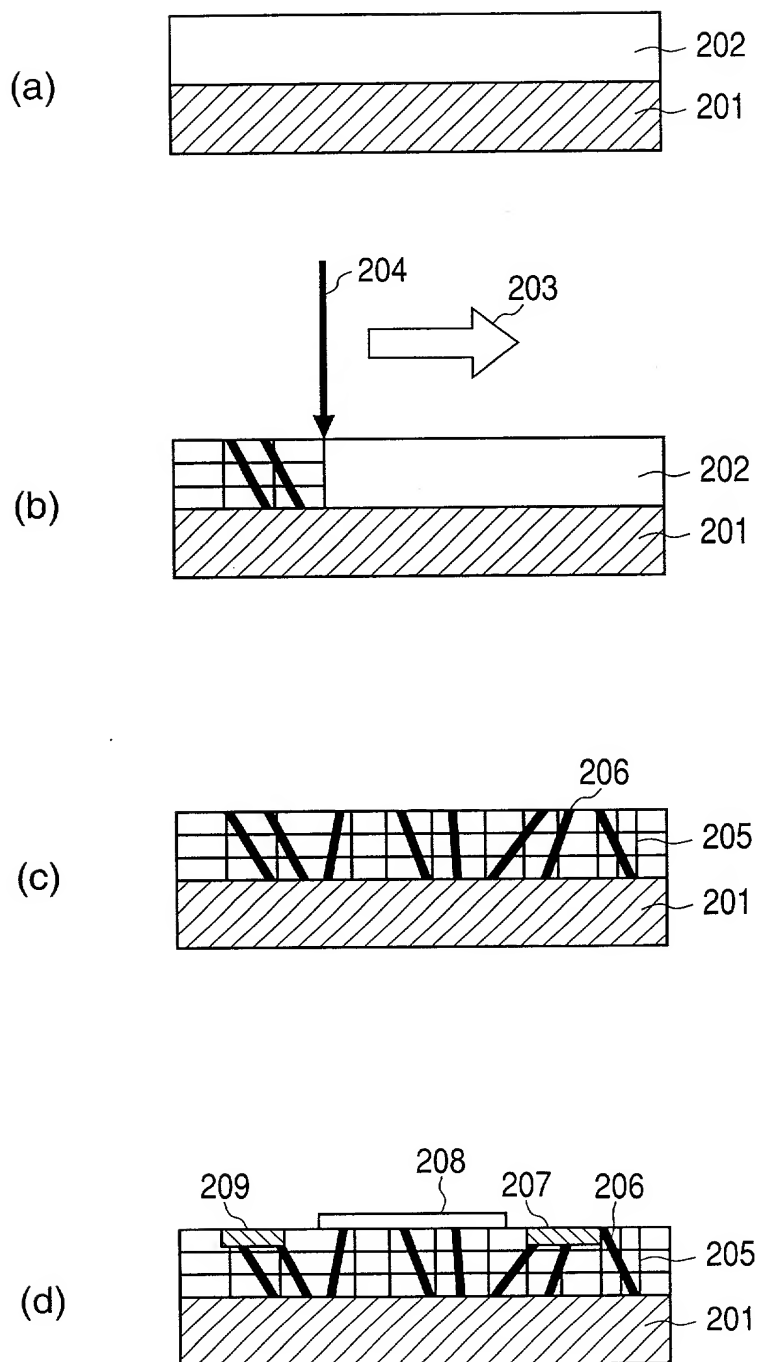


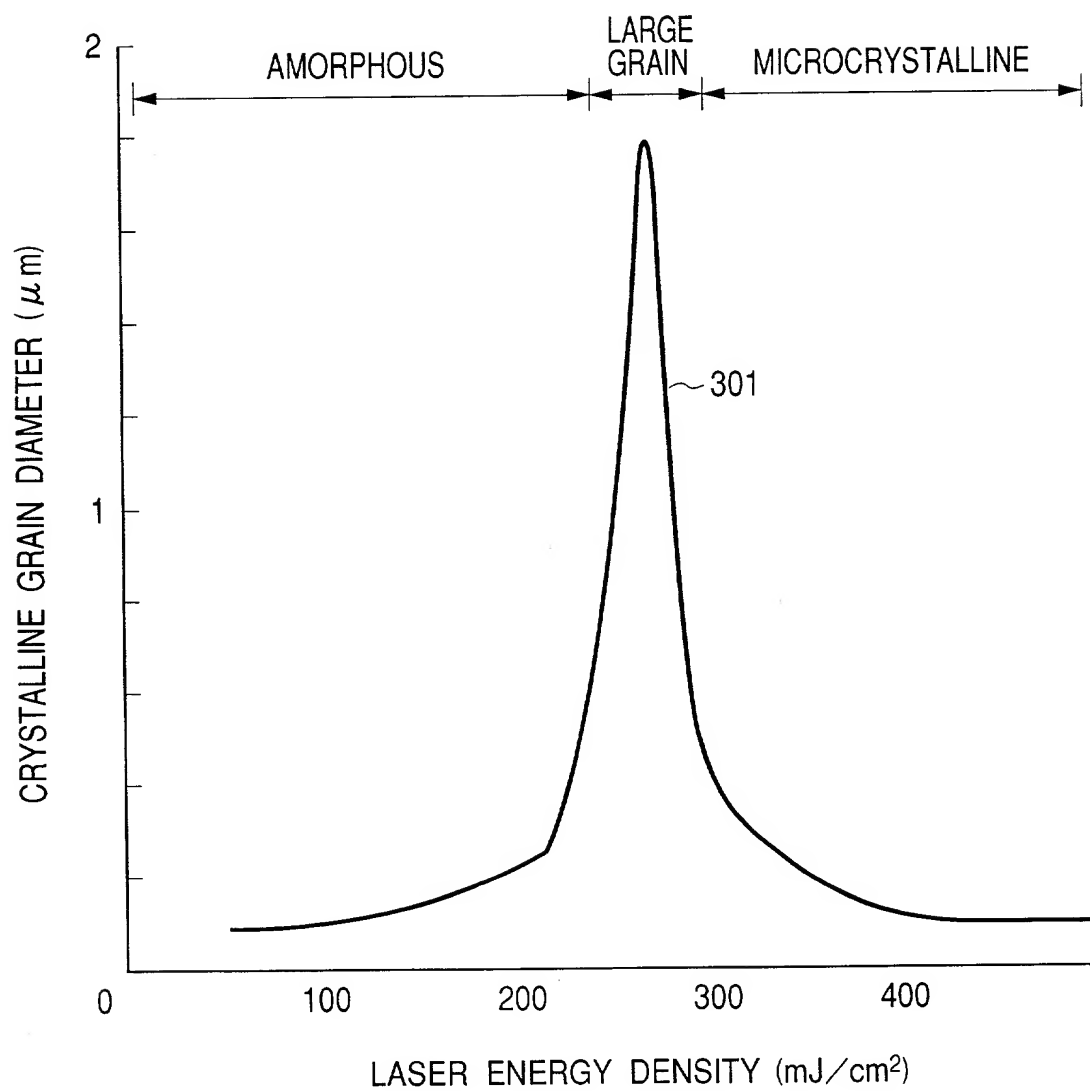
FIG. 16

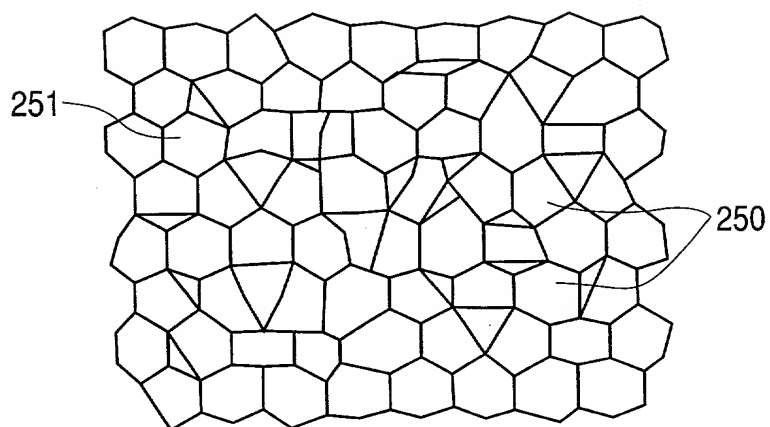


**FIG. 17**

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FIG. 18



**FIG. 19**

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国際事務局



(43) 国際公開日  
2001年1月4日 (04.01.2001)

PCT

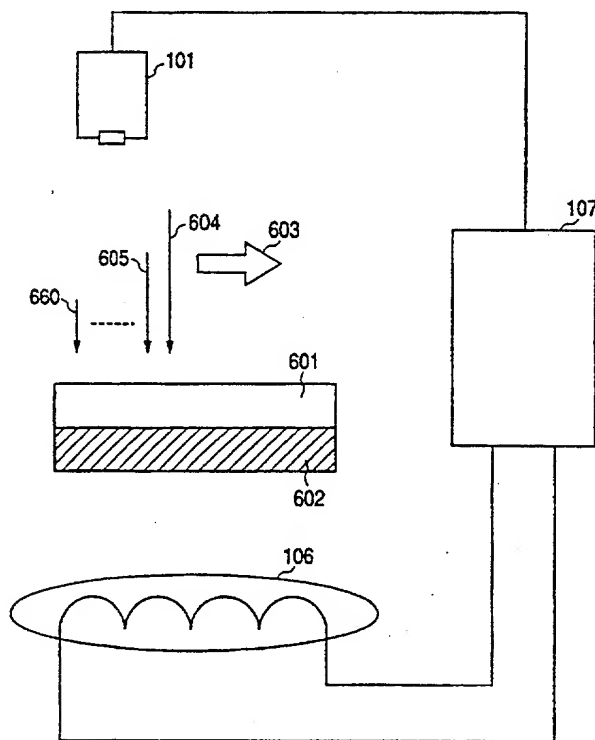
(10) 国際公開番号  
WO 01/01464 A1

- (51) 国際特許分類: H01L 21/20, 29/786 (72) 発明者; および  
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(22) 国際出願日: 2000年6月23日 (23.06.2000) (KIMURA, Yoshinobu) [JP/JP]. 賀茂尚広 (KAMO,  
(25) 国際出願の言語: 日本語 Takahiro) [JP/JP]. 金子好之 (KANEKO, Yoshiyuki)  
(26) 国際公開の言語: 日本語 [JP/JP]; 〒185-8601 東京都国分寺市東恋ヶ窪一丁目  
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(81) 指定国 (国内): CN, JP, KR, US.  
(84) 指定国 (広域): ヨーロッパ特許 (AT, BE, CH, CY, DE,  
DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

[続葉有]

(54) Title: POLYSILICON SEMICONDUCTOR THIN FILM SUBSTRATE, METHOD FOR PRODUCING THE SAME, SEMI-  
CONDUCTOR DEVICE, AND ELECTRONIC DEVICE

(54) 発明の名称: 多結晶半導体薄膜基板、その製造方法、半導体装置および電子装置



(57) Abstract: A method for producing a semiconductor device by forming an amorphous semiconductor film on an insulating substrate, irradiating the amorphous semiconductor film with a laser beam to crystallize the amorphous semiconductor film and thereby to form a polycrystalline semiconductor film, and fabricating a transistor in the polycrystalline semiconductor film, wherein the back of the insulating substrate or the amorphous semiconductor film is irradiated with ultraviolet radiation to heat the amorphous semiconductor film to a temperature under the melting point, the amorphous semiconductor film is irradiated with a laser beam with a shape selection suitable laser beam energy density  $E_c$  at which crystal grains whose the number of nearest crystal grains is six are formed the most so as to change the amorphous semiconductor film to a polycrystalline semiconductor film, and a transistor is fabricated in the polycrystalline semiconductor film. A thin film transistor capable of operating at high speed can be fabricated with high yield.

[続葉有]

WO 01/01464 A1



添付公開書類:  
— 国際調査報告書

2文字コード及び他の略語については、定期発行される各PCTガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(57) 要約:

絶縁性基板の表面に非晶質半導体膜を形成した後、前記非晶質半導体膜にレーザ光を照射して前記非晶質半導体膜を結晶化して多結晶半導体薄膜を形成し、その後前記多結晶半導体薄膜にトランジスタを形成する半導体装置の製造方法であって、前記絶縁性基板裏面または前記非晶質半導体膜に紫外線を照射して前記非晶質半導体膜を溶融温度以下に加熱するとともに、最近接結晶粒数が6の結晶粒が最も多く形成される形状選択好適レーザエネルギー密度 $E_c$ のレーザ光を前記非晶質半導体膜面に照射して多結晶半導体薄膜に変換させ、その後前記多結晶半導体薄膜にトランジスタを形成する。

高い歩留まりでかつ高速動作の薄膜トランジスタを作製できる。

2052507.032503

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# Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

10

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発明者の署名	日付	Inventor's signature	<i>Yoshinobu Kimura</i> 11/29/2001
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国籍		Citizenship	Korea
私書箱		Post Office Address	c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

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(Supply similar information and signature for second and subsequent joint inventors.)



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国籍		Citizenship Japan	
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第三共同発明者名	3-00	Full name of third joint inventor, if any Yoshiyuki KANEKO	
第三共同発明者の署名	日付	Third inventor's signature Yoshiyuki Kaneo	Date 12/5/2001
住所		Residence Hachioji, Japan JPX	
国籍		Citizenship Japan	
私書箱		Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	
第四共同発明者名		Full name of fourth joint inventor, if any	
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住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第五共同発明者名		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

(第六以降の共同発明者についても同様に記載し、署名をすること)

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N70555

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## Declaration and Power of Attorney For Patent Application

### 特許出願宣言書及び委任状

### Japanese Language Declaration

### 日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

POLYCRYSTALLINE SEMICONDUCTOR THIN FILM

SUBSTRATE, MANUFACTURING METHOD OF THE SAME,

SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約  
国際出願番号を \_\_\_\_\_ とし、  
(該当する場合) \_\_\_\_\_ に訂正されました。

☒ was filed on 23 / June / 2000  
as United States Application Number o  
PCT International Application Number  
PCT/JP00/04141 and was amended on  
\_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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## Japanese Language Declaration

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私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国外の国の少なくとも一か国を指定している特許協力条約365(a)項に基づき国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

## Prior Foreign Application(s)

外国での先行出願

11-181559	Japan
(Number)	(Country)
(番号)	(国名)
(Number)	(Country)
(番号)	(国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

28 / June / 1999

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.